REMARKS

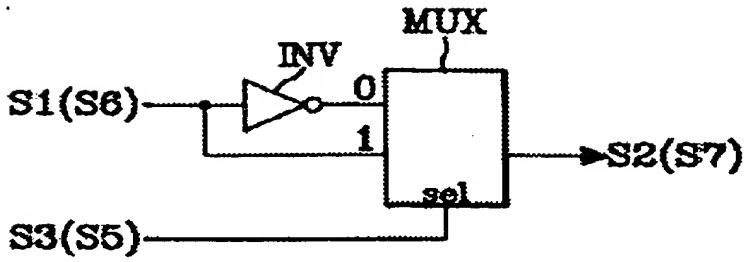
Pursuant to the above-noted Office Action, claims 1-13 were rejected. In particular, claim 1 was rejected under 35 U.S.C. §102(e) give Hwang, claims 6-9 and 11-13 were rejected under 35 U.S.C. §102(e) given Heitschel et al., claim 10 was rejected under 35 U.S.C. §102(e) give Holmes, claim 2 was rejected under 35 U.S.C. §103(a) given Hwang in view of Holmes, claims 3 and 4 were rejected under 35 U.S.C. §103(a) given Hwang in view of Schulze, claim 8 appears to have been rejected under 35 U.S.C. 103(a) give Hwang in view of Schulze, claim 13 appears to have been rejected under 35 U.S.C. 103(a) given Hwang in view of Schulze, and claim 5 was rejected under 35 U.S.C. §103(a) given Hwang in view of Freen. These rejections are respectfully traversed and reconsideration kindly requested.

Claim 1 was rejected under 35 U.S.C. 102(e) as being anticipated by Hwang. Prior to discussing the Examiner's contentions, the applicant believes it would be helpful to first briefly characterize the Hwang reference.

U.S. Patent No. 5,907,795 ("Hwang") discloses a battery saving radio paging signal transmitting and receiving system. According to Hwang, a pager may be either a local area service subscriber or a wide area service subscriber. Both types of subscriber can share a common reception carrier and both types of subscriber services use the same POCSAG signaling, including the corresponding POCSAG bit pattern (FIG. 4 of Hwang is particularly illustrative of the specific details of this shared POCSAG signaling). Hwang provides further elaboration regarding his bit pattern as follows:

> One POCSAG code is comprised of 576 bits of preamble data and several intervals of batch data in a continuous arrangement. The preamble data is a code in which logical 1's and 0's are alternately repeated for 576 bits (i.e., a redundancy code). One POCSAG code includes between 30 and 60 batches of data. One batch of data includes 32 bits of wordsync data and 8 frames of data, wherein each frame includes 64 bits. In FIG. 4, the wordsync data contains 32 bits of data (i.e., "7CD215D8" in hexidecimal and "01111100 11010010000101011101100" in binary). Also, each frame of data includes 64 bits of data (i.e., 32 bits of an address codeword and 32 bits of a message codeword). Accordingly, one batch of data includes 544 bits. That is, 17 words with each word having 32 bits (i.e., 17 words.times.32 bits=544 bits). [Column 4, line 58 - column 5, line 5.]

To allow for differentiation as between signals intended for local area and wide area subscribers, Hwang inverts data intended for wide area subscribers. Hwang's pager receivers are provided with a controllable inverting unit as shown in his FIG. 3 (reproduced below for the convenience of the Examiner) to permit compatible decoding of wide area data that has been so inverted.



Hwang does not teach or suggest the use of any protocol that would accommodate varying bit lengths, particularly for codes that correspond to receiver actuation signals.

Claim 1, however, provides for both different codes and different bit patterns wherein at least some of the different bit patterns differ from one another with respect to packet length. Claim 1 is therefor distinguishable from Hwang in at least this one regard.

Claims 6-9 and 11-13 were rejected under 35 U.S.C. §102(e) as being anticipated by Heitschel et al.. Again, the applicant believes it will be helpful to first briefly characterize the Heitschel et al. reference.

U.S. Patent No. Re. 36,703 ("Heitschel") discloses a coding system for multiple transmitters and a single receiver for a garage door opener. Heitschel provides a garage door opener having a receiver that can receive wireless operating signals from a plurality of remote transmitters. Since each transmitter can have a different corresponding code, Heitschel provides a mechanism for allowing the receiver to learn such codes for each authorized transmitter. In particular, and as shown in FIG. 2 (reproduced below for the convenience of the Examiner), a first switch (22) can be placed between an "operate" mode for normal operations and a "program" mode for learning a transmitter code. A second switch (23) identifies the transmitter for purposes of correlating the learned code with a given authorized transmitter. In Heitschel's illustrated embodiment, up to 5 transmitters can have their corresponding codes learned in this fashion.

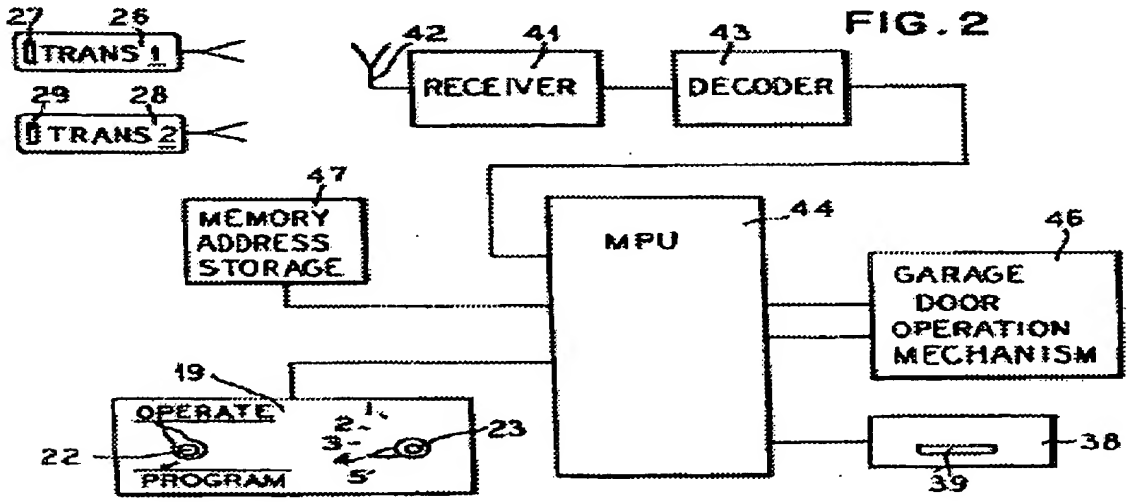
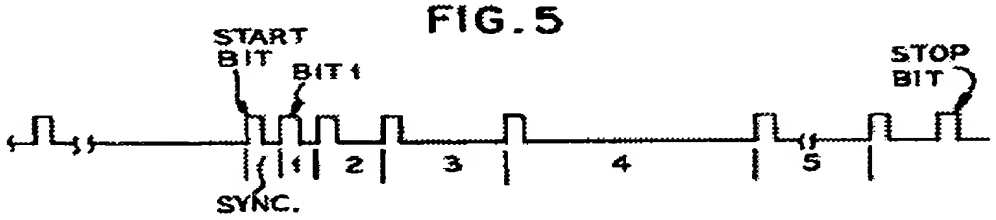


FIG. 2

Heischel's disclosed codes, although potentially different from transmitter to transmitter, use identical bit patterns as explained in the following text and illustrated in FIG. 5 (presented below for the convenience of the Examiner):

FIG. 5



> In the illustrated embodiment, the receiving unit can respond to up to five different transmitters which have five different transmitting codes. FIG. 5 illustrates the code utilized in which the bit times are nominally 0.5 milliseconds for example. The data times are nominally 1, 2, 3 or 4 milliseconds.
>
> The sync pulse is a unit measure of time. Each datum is measured with respect to the sync pulse and each datum can be 1, 2, 3 or 4 times the length of the sync pulse. The timing is from the riding edge to rising edge of adjacent pulses. Using 10 data bits the number of codes which is available is in excess of one million codes. [Column 3, lines 19-30.]

Heitschel does not teach or suggest that multiple bit patterns can or should be accommodated. Further, Heitschel does not teach that any user interface be provided to permit selection of codes or bit patterns. In fact, Heitschel specifically teaches away from selecting codes in such a fashion. For example, Heitschel states:

> This invention eliminates the requirement that binary switches be set in the transmitter or receiver as is done in systems of the prior art to establish a code to which the receiver will respond . . . . [Column 4, lines 15-18.]

Claim 6, however, provides for both a plurality of different codes and different bit patterns wherein at least some of the bit patterns differ from one another with respect to packet length. As before, such a notion is neither taught nor suggested by the Heitschel reference. Independent claim 6 is therefor readily distinguished form the Heitschel reference.

Claims 7, 8 and 9 are dependent upon claim 6, which claim has just been shown allowable. In addition, these claims introduce additional substantive content that is neither taught nor disclosed by these references. For example, claim 7 specifies the use of a user selectable input device comprising a multi-position switch to determine a particular code to be received as an actuation signal. Heitschel, although having a multi-position switch, provides no such associated feature. The same can be said for claim 8 which specifies a dual in-lined packaged switch that is used to determine a particular bit sequence to be received as an actuation signal and claim 9 wherein the code and bit sequence selections of claim 7 and 8 are processed to further facilitate the operation of the receiver circuitry.

Claim 11 is a method claim and specifies adjusting receiver circuitry to receive a particular code at a particular frequency based on the position of both a plurality of input devices and output

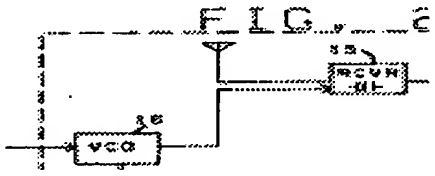
from a microprocessor. Heitschel teaches two switches, that, for purposes of argument, might be considered multiple input devices, which nevertheless are not used to select a particular code and/or to thereby cause a receiver circuit to receive a particular code at a particular frequency based on the position of those switches. Claim 11 is therefor readily distinguished from the teachings of Heitschel.

Claims 12 and 13 are dependent upon claim 11, which claim has been shown allowable above. In addition, these claims set forth specific details regarding selection of a specific code and determination of a particular bit pattern via the multiple input devices, which details are also neither taught nor suggested by the Heitschel reference.

Claim 10 was rejected under 35 U.S.C. §102(e) as being anticipated by Holmes. Again, prior to discussing the Examiner's contentions, the applicant believes it would be helpful to first briefly characterize the Holmes reference.

U.S. Patent No. 5,262,769 ("Holmes") discloses a programmed scanning pager receiver. As shown in FIG. 2A of that reference (a portion of which is reproduced below for the convenience of the Examiner) this pager receiver includes an RF detecting stage 15. In the words of Holmes:

> The RF detecting stage 15 is a conventional circuit and includes in series, a varactor diode tuned antenna matching circuit, an isolation amplifier, a band pass filter, a summing circuit, an intermediate frequency filter and a first detector stage, the output of which is connected to the input of the SCA detector 18. [Column 7, lines 31-37.]



Holmes therefore teaches the use of a varactor diode. Varactor diodes, of course, exhibit a variable capacitance that changes in correlation to a biasing voltage as is applied thereto. The varactor diode of Holmes serves an integral purpose and is not used to switch other discrete elements in and out of an operating relationship with respect to other circuits or components. Holmes further does not teach the use of a signal diode (as versus a varactor diode) that connects to other discrete circuit elements and that is used to switch such other circuit elements in and out with respect to a bandpass filter or any other component or circuit.

The Examiner contends that Holmes discloses provision of a signal diode that can connect additional discreet component to a band pass filter. This contention is inaccurate as shown above. Rather, Holmes teaches the use of a varactor diode to, in and of itself, offer a variable capacitance for known tuning purposes. Claim 10, however, specifically requires provision of a signal diode that can be used to connect additional discrete components to a

band pass filter. Since Holmes has neither such a diode nor any additional discrete components to be connected by any other means, the applicant respectfully submits that claim 10 is readily distinguished from the Holmes reference.

Claim 2 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Hwang in view of Holmes. Claim 2 is dependent upon claim 1, which claim has been shown allowable above. In addition, claim 2 sets forth additional details regarding provision of a signal diode capable of adding and removing discrete components from a band pass filter. The Examiner has thought to combine Holmes with the Hwang reference. Holmes, however, as noted above, does not teach the use of a signal diode that is capable of adding and removing discreet components from a band pass filter, nor the use of any other component to add or remove discrete components from a band pass filter. Therefor, claim 2 is readily distinguishable from the combined reference in this manner as well.

Claim 3 and 4 were rejected under 35 U.S.C. §103(a) given Hwang in view of Schulze. Claims 3 and 4 are dependent upon claim 2 (and ultimately claim 1) which claims were shown allowable above. In addition, these claims set forth additional specificity with respect to the selection of a multi-position switch for selecting a code and a DIP switch for selecting a particular bit pattern. A combination of Schulze with Hwang fails to achieve the structure of the claims, in part because Hwang fails to teach provision of a code in this fashion or the provision of a bit pattern from amongst a plurality of different bit patterns wherein the bit patterns differ from one another with respect to packet length. Therefor, these claims are readily distinguished from the references of record.

Claim 8 has been rejected, apparently under 35 U.S.C. §103(a) given Hwang in view of Schulze. Claim 8 is dependent upon claim 7 and ultimately upon claim 6, which claims have been shown allowable above. In addition, claim 8 sets forth additional detail regarding use of a dual inline packaged switch to determine a particular bit sequence. Again, considered individually or in combination, Hwang and Schulze do not teach or suggest any such structure.

Claim 13 was additionally rejected, apparently under 35 U.S.C. §103(a) given Hwang in view of Schulze. Claim 13 is dependent upon claim 12 which depends upon claim 11, both of which claims were shown allowable above. In addition, claim 13 introduces additional subject matter, including a dual inline packaged switch which determines bit pattern to be received as a receiver actuating signal. This structure is not found in either Hwang or Schulze, alone or in combination. Claim 13 is therefor readily distinguished from these references of record.

Lastly, claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over Hwong in view of Freen. As noted earlier, however, Hwong fails to teach or suggest the use of a plurality of different codes and different bit patterns wherein at least some of the bit patterns differ from one another with respect to packet length. Freen also fails to provide such an approach. Since such

elements are included in claim 5, claim 5 is readily distinguished from Hwong and Freen alone or in combination, for at least these grounds.

There being no other objections or rejections, the applicant respectfully submits that claim 1-13 may be passed to allowance.

Respectfully submitted
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PATENT APPLICATION
ATTORNEY DOCKET
NO. 68702

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Nguyen et al.

Application No.: 09/557,690

Title: Method and Apparatus for Receiving a Plurality of Different Codes at a Plurality of Different Frequencies

Filed: April 25, 2000

Group Art Unit: 2683

Examiner: Rampuria, S.

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on this date.

10/1/02
Date

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AMENDMENT APPENDIX

Honorable Commissioner of Patents
and Trademarks
Attention: Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Pursuant to 37 C.F.R. § 1.121, as amended effective 7 November, 2000, Applicants present herewith marked-up text of the claims of this application as amended by the foregoing amendment:

IN THE CLAIMS:

1. (Amended once) A receiver capable of receiving a plurality of different codes at a plurality of different frequencies, comprising:

an input device for selection among a plurality of different codes and a plurality of different bit patterns wherein at least some of the plurality of different bit patterns differ from one another with respect to packet length;

an antenna for receiving a receiver actuation signal;

digital frequency control circuitry;

a controller for comparing said received receiver actuation signal to said code and bit pattern selections; and

output circuitry for responding to the receipt of a receiver actuation signal that matches said code and bit pattern selections.

5. (Amended once) A super-regenerative receiver capable of receiving a plurality of different codes at a plurality of different frequencies, comprising:

an input device for selection among a plurality of different codes and a plurality of different bit patterns wherein at least some of the plurality of different bit patterns differ from one another with respect to packet length;

an antenna for receiving a receiver actuation signal;

digital frequency control circuitry;

a controller for comparing said received receiver actuation signal to said code and bit pattern selections; and

output circuitry for responding to the receipt of a receiver actuation signal that matches said code and bit pattern selections.

6. (Amended once) A radio frequency receiver for receiving a plurality of actuation signals from a movable barrier operator transmitter, each receiver being capable of receiving a plurality of coded signals comprising:

a plurality of different codes; and

different bit patterns wherein at least some of the bit patterns differ from one another with respect to packet length;

at a plurality of different frequencies, comprising:

first and second user-selectable input devices for selecting a specified code and a specified [frequency] bit pattern for receiving said actuation signals;

a controller coupled to said input devices for processing said code and [frequency] bit pattern selections and outputting data responsive to said input; and

receiver circuitry responsive to said controller output data for receiving particular actuation signals at one frequency and receiving particular other actuation signals at another frequency.

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